AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An array substrate for use in an IPS-LCD device, comprising:

a gate line over a substrate and disposed in a first direction;

a common line over the substrate and disposed in the first direction next to the gate line;

a data line over the substrate and disposed in a second direction substantially perpendicularly crossing both the gate line and the common line to define a pixel region;

a thin film transistor at a crossing of the gate and data lines;

a pixel electrode in the pixel region, the pixel electrode having a plurality of pixel fingers and a pixel horizontal portion; and

a common electrode in the pixel region, the common electrode having a plurality of common fingers extending from the common line parallel with the pixel fingers,

wherein each of the common fingers has a gentle slope outline at a portion where the common finger meets the pixel finger,

wherein the gentle slope outline includes a first portion, a second portion and a third portion having different slopes from one another, and

wherein the first portion is at an angle with respect to the common fingers, wherein the angle is between about 70 degrees and about 90 degrees.

2. (Original) The array substrate according to claim 1, wherein the thin film transistor includes a gate electrode connected to the gate line, an active layer, a source electrode connected to the data line, and a drain electrode connected to the pixel electrode.

3. (Original) The array substrate according to claim 1, wherein the pixel fingers and the common fingers have zigzag shapes.

4. (Original) The array substrate according to claim 4, wherein a bent angle of the zigzag shapes is about ±1-30 degrees with respect to an alignment direction of a liquid crystal layer.

5. (Original) The array substrate according to claim 1, wherein the plurality of pixel fingers are disposed in the second direction.

6. (Original) The array substrate according to claim 1, wherein the pixel horizontal portion connects the plurality of pixel fingers and is disposed in the first direction.

7. (Original) The array substrate according to claim 6, wherein the pixel horizontal portion is electrically connected with the drain electrode of the thin film transistor.

8. (Original) The array substrate according to claim 1, wherein the common line and the common electrode are formed as one united body.

9. (Original) The array substrate according to claim 1, wherein the pixel fingers and the pixel horizontal portion are formed as one united body.

10. (Original) The array substrate according to claim 1, wherein the common fingers do not meet the pixel horizontal portion in the pixel region.

11. (Cancelled)

12. (Currently Amended) The array substrate according to claim [[11]] 1, wherein the first portion is substantially perpendicular to the data line.

13. (Cancelled)

14. (Currently Amended) The array substrate according to claim [[11]] 1, wherein the first portion is at an angle of about 70 degrees with respect to the pixel fingers.

15. (Currently Amended) The array substrate according to claim [[11]] 1, wherein the second portion is at an angle of about 160 degrees with respect to the first portion.

16. (Currently Amended) The array substrate according to claim [[11]] 1, wherein the third portion is at an angle of about 130 degrees with respect to the second portion.

17. (Currently Amended) The array substrate according to claim [[1q]] 1, wherein the second portion and the third portion meet at an obtuse angle.

18. (Currently Amended) The array substrate according to claim [[11]] 1, wherein the vertices between the first portion, the second portion and the third portion are rounded.

19. (Currently Amended) A method of fabricating an array substrate for use in an IPS-LCD device, comprising:

forming a gate line over a substrate and disposed in a first direction;

forming a common line over the substrate and disposed in the first direction next to the gate line;

forming a data line over the substrate and disposed in a second direction substantially perpendicularly crossing both the gate line and the common line to define a pixel region;

providing a thin film transistor at a crossing of the gate and data lines;

forming a pixel electrode in the pixel region, the pixel electrode having a plurality of pixel fingers and a pixel horizontal portion; and

forming a common electrode in the pixel region, the common electrode having a plurality of common fingers extending from the common line parallel with the pixel fingers,

wherein each of the common fingers has a gentle slope outline at a portion where the common finger meets the pixel finger,

wherein the gentle slope outline includes a first portion, a second portion and a third portion having different slopes from one another, and

wherein the first portion is at an angle with respect to the common fingers, wherein the angle is between about 70 degrees and about 90 degrees.

20. (Original) The method of fabricating an array substrate of claim 19, wherein the thin film transistor includes a gate electrode connected to the gate line, an active layer, a source electrode connected to the data line, and a drain electrode connected to the pixel electrode.

21. (Original) The method of fabricating an array substrate according to claim 19, wherein the pixel fingers and the common fingers have zigzag shapes.

22. (Original) The method of fabricating an array substrate according to claim 21, wherein a bent angle of the zigzag shapes is about ±1-30 degrees with respect to an alignment direction of a liquid crystal layer.

23. (Original) The method of fabricating an array substrate according to claim 19, wherein the plurality of pixel fingers are disposed in the second direction.

24. (Original) The method of fabricating an array substrate according to claim 19, wherein the pixel horizontal portion connects the plurality of pixel fingers and is disposed in the first direction.

25. (Original) The method of fabricating an array substrate according to claim 24, wherein the pixel horizontal portion is electrically connected with the drain electrode of the thin film transistor.

26. (Original) The method of fabricating an array substrate according to claim 19, wherein the common line and the common electrode are formed as one united body.

27. (Original) The method of fabricating an array substrate according to claim 19, wherein the pixel fingers and the pixel horizontal portion are formed as one united body.

28. (Original) The method of fabricating an array substrate according to claim 19, wherein the common fingers do not meet the pixel horizontal portion in the pixel region.

29. (Cancelled)

30. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the first portion is substantially perpendicular to the data line.

31. (Cancelled)

32. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the first portion is at an angle of about 70 degrees with respect to the common fingers.

33. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the second portion is at an angle of about 160 degrees with respect to the first portion.

34. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the third portion is at an angle of about 130 degrees with respect to the second portion.

35. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the second portion and the third portion meet at an obtuse angle.

36. (Currently Amended) The method of fabricating an array substrate according to claim [[29]] 19, wherein the vertices between the first portion, the second portion and the third portion are rounded.